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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,237	02/27/2004	Thomas A. Bos	51755/JEJ/F283	7977

7590 05/13/2005

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EXAMINER	
HAROON, ADEEL	

ART UNIT	PAPER NUMBER
2685	

DATE MAILED: 05/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/789,237	BOS ET AL.	
	Examiner	Art Unit	
	Adeel Haroon	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-29 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-29 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-3, 5-9, 18-22, and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Merenda (U.S. 6,879,192).

With respect to claim 1, Merenda discloses a sub-harmonic mixer in figure 4c that comprises an input, node 121, for receiving a first signal having a first frequency and a second signal having a second frequency and an output, node 123, for outputting a third signal having a third frequency (Column 8, lines 37-42). Merenda teaches having at least one diode ring array it having a plurality of diode rings arranged in

parallel in figure 4c (Column 8, lines 37-42). Merenda teaches that an even harmonic mixer, diode ring array, doubles the LO, the second signal, producing a fourth signal which is multiplied to the first signal, either RF or IF, to generate the third signal (Column 1, line 64 – Column 2, line 4).

With respect to claim 2, Merenda discloses a sub-harmonic diode mixer in a circuit in figure 4a. Merenda teaches that the input to the diode ring, element number 92, can be coupled to ground (Column 7, lines 39-43). Merenda also teaches that the diode ring, element number 92, can be connected to ground instead of the output (Column 7, lines 15-18).

With respect to claim 3, Merenda teaches that the diode ring array is coupled between the input, node 121, and the output, element number 123 (Column 8, lines 39-43).

With respect to claims 5 and 6, Merenda teaches that the sub-harmonic mixer is used transceivers so it is used as an up-conversion mixer where the first frequency would be an IF frequency, the second frequency is an LO frequency, and the third frequency, which is higher than the first frequency is an RF frequency (Column 7, lines 39-43).

With respect to claims 7 and 8, Merenda teaches that the sub-harmonic mixer is used transceivers so it is used as an down-conversion mixer where the first frequency, which is higher than the third frequency, would be an RF frequency, the second frequency is an LO frequency, and the third frequency, is an IF frequency (Column 7, lines 39-43).

With respect to claim 9, a sub-harmonic mixer used in a transceiver thus it can be a transmitter (Column 7, lines 39-43). Merenda discloses in figure 4c, a sub-harmonic mixer having at least one diode ring array with it having a plurality of diode rings arranged in parallel (Column 8, lines 37-42). Merenda teaches receiving an IF signal in the mixer and translating the IF signal to a transmission signal, RF signal, having a transmission frequency (Column 8, lines 37-42). Merenda discloses an oscillator for generating a local oscillator (LO) frequency signal having an LO signal (Column 7, lines 39-43). Merenda teaches that an even harmonic mixer, a diode ring array, when used as a receiver doubles the LO, the second signal, which is multiplied to the RF signal to generate the IF signal (Column 1, line 64 – Column 2, line 4). Since the mixer can also be used in a transmitter, it is considered inherent that the diode ring array doubles the LO, the second signal, which is multiplied to the IF signal to generate the transmission signal.

With respect to claim 18, Merenda discloses using surface mount, diode rings; therefore it is considered inherent that the sub-harmonic mixer is implemented on a MMIC chip since surface mount diodes are used on MMIC chips (Column 8, lines 59-63).

With respect to claim 19, Merenda discloses a sub-harmonic diode mixer in a circuit in figure 4a. Merenda teaches that the input to the diode ring, element number 92, can be coupled to ground (Column 7, lines 39-43). Merenda also teaches that the diode ring, element number 92, can be connected to ground instead of the output (Column 7, lines 15-18).

With respect to claim 20, Merenda teaches that the diode ring array is coupled between the input, node 121, and the output, element number 123 (Column 8, lines 39-43).

With respect to claim 21, Merenda teaches that when the harmonic mixer is used in receiving the receiving frequency can include both the sum and the difference of twice the LO frequency and the RF frequency (Column 1, line 64 – Column 2, line 4). Therefore, it is considered inherent that when the mixer is used in a transmitter, the transmission frequency can include both the sum and the difference of twice the LO frequency and the IF frequency.

With respect to claim 22, Merenda discloses a method of generating a transmission signal having a transmission frequency from an intermediate frequency signal. Merenda teaches generating a local oscillator (LO) frequency signal having a LO signal (Column 7, lines 39-43). Merenda teaches using a sub-harmonic mixer of figure 4c that includes at least one diode ring array with each having a plurality of diode rings arranged in parallel (Column 8, lines 37-42). Merenda teaches that when using the mixer in a receiver, multiplying the signal having a twice the LO frequency to the RF signal to generate the intermediate signal (Column 1, line 64 – Column 2, line 4). Since Merenda shows that the mixer can be used both as a transmitter and receiver, transceiver (Column 7, lines 39-43), it is considered inherent that the mixer would multiply the signal having a twice the LO frequency to the IF signal to generate the transmission signal.

With respect to claim 29, With respect to claim 9, a sub-harmonic mixer used in a transceiver thus it can be a receiver (Column 7, lines 39-43). Merenda discloses in figure 4c, a sub-harmonic mixer having at least one diode ring array with it having a plurality of diode rings arranged in parallel (Column 8, lines 37-42). Merenda teaches receiving a transmission signal in the mixer and translating the transmission signal to an IF signal, RF signal, having a transmission frequency (Column 8, lines 37-42). Merenda discloses an oscillator for generating a local oscillator (LO) frequency signal having an LO signal (Column 7, lines 39-43). Merenda teaches that an even harmonic mixer, a diode ring array, doubles the LO, the second signal, which is multiplied to the RF signal to generate the IF signal (Column 1, line 64 – Column 2, line 4).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4, 12-16, 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merenda in view of Joshi (U.S. 5,416,449).

With respect to claim 4, the sub-harmonic mixer of Merenda is described above in the discussion of claim 1. Merenda does not disclose using two diode ring arrays, thus making it two separate mixers. However, Joshi teaches using two harmonic

mixers, element numbers 20 and 30 (Column 6, lines 37-42). The use of two mixers, diode ring arrays, forms an image rejection mixer. Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to use Merenda's sub-harmonic mixer as the two harmonic mixers in Joshi's quadrature image rejection mixer system in order to eliminate interference.

With respect to claim 12, the transmitter of Merenda is described above in the discussion of claim 9. Merenda does not disclose using two diode ring arrays, thus making it two separate mixers. However, Joshi teaches using two harmonic mixers, element numbers 20 and 30 (Column 6, lines 37-42). The use of two mixers, diode ring arrays, forms an image rejection mixer. Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply Joshi's technique of using two harmonic mixers to Merenda's transmitter in order to form an image rejection mixer and thus eliminating interference.

With respect to claim 13, the modified transmitter of Merenda and Joshi is described above in the discussion of claim 12. Merenda does not disclose a power divider. Joshi further discloses in figure 1 using a power divider, element number 40, for dividing the LO frequency signal to generate two divided LO frequency signals, and providing the two divided LO frequency signals to the two diode ring arrays, element numbers 20 and 30, respectively (Column 5, line 67 – Column 6, line 6). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to add Joshi's power divider to the modified transmitter of Merenda and Joshi in order to have the capability of modulating two signals at the same time.

With respect to claim 14, the modified transmitter of Merenda and Joshi is described above in the discussion of claim 12. Merenda does not disclose a hybrid for generating two quadrature IF signals. Joshi describes the use of a first and second quadrature IF signals, element numbers 28 and 38, that are provided to the two diode ring array mixers, element numbers 20 and 30 (Column 6, lines 26-29). A hybrid is necessary to produce these the first and second quadrature IF signals; hence, a hybrid must be present. Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to add Joshi's hybrid system to generate two quadrature IF signals to the modified transmitter of Merenda and Joshi in order to have the capability of modulating both quadrature signals of the same IF signal.

With respect to claim 15, the modified transmitter of Merenda and Joshi is described above in the discussion of claim 12. Merenda does not disclose a hybrid for combining the outputs of the diode ring arrays. However, Joshi further discloses a hybrid, element number 50, for combining outputs of the two-diode ring arrays to generate the transmission signal (Column 7, lines 17-24). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to add Joshi's hybrid system to generate two quadrature IF signals to the modified transmitter of Merenda and Joshi in order to have the capability of modulating both quadrature signals of the same IF signal and then combining the outputs.

With respect to claim 16, the transmitter of Merenda is described above in the discussion of claim 9. Merenda does not disclose a filter as recited in the claim.

However, Joshi discloses a filter, element number 70, coupled to the output port of a sub-harmonic mixer (Column 7, lines 31-34).

With respect to claim 24, Merenda's method is described above in the discussion of claim 22. Merenda does not disclose using two diode ring arrays, thus making it two separate mixers. However, Joshi teaches using two harmonic mixers, element numbers 20 and 30 (Column 6, lines 37-42). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply Joshi's technique of using two harmonic mixers to Merenda's method in order to be able to up-convert both quadratures of the IF signal.

With respect to claim 25, the modified method of Merenda and Joshi is described above in the discussion of claim 24. Merenda does not disclose a method for dividing the LO frequency signal. However, Joshi discloses a method for dividing the LO frequency signal using a power divider, element number 40, to generate two divided LO frequency signals, and providing the two divided LO frequency signals to the two diode ring arrays, element numbers 20 and 30, respectively (Column 5, line 67 – Column 6, line 6). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply Joshi's technique of dividing the LO frequency signal to the modified method of Merenda and Joshi in order to be able to up-convert both quadratures of the IF signal.

With respect to claim 26, the modified method of Merenda and Joshi is described above in the discussion of claim 24. Merenda does not disclose a method for combining the outputs of the diode ring arrays. However, Joshi discloses a method for

combining outputs of the two-diode ring arrays to generate the transmission signal (Column 7, lines 17-24). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply Joshi's technique of combining the outputs to the modified method of Merenda and Joshi in order to be able to up-convert both quadratures of the IF signal.

With respect to claim 27, the modified method of Merenda and Joshi is described above in the discussion of claim 24. Merenda does not disclose a method for generating the first and second quadrature IF signals. However, Joshi discloses a method for generating the first and second quadrature IF signals, element numbers 28 and 38, and providing them to the two diode ring arrays, element numbers 20 and 30, respectively (Column 6, lines 26-29). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply Joshi's technique of generating two quadrature IF signals to the modified method of Merenda and Joshi in order to be able to up-convert both quadratures of the IF signal.

With respect to claim 28, Merenda's method is described above in the discussion of claim 22. Merenda does not disclose a filtering method. However, Joshi teaches filtering a signal at the output port of the sub-harmonic mixer (Column 7, lines 29-36). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply Joshi's filtering technique to Merenda's method in order to enhance the quality of the method by isolating the desired signal.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Merenda in view of Moe et al. (U.S. 5,239,685). The transmitter of Merenda is described above in the discussion of claim 9. Merenda does not disclose a LO amplifier. However, Moe et al. discloses a transmitter on a MMIC that utilizes a LO amplifier, element number 75, for amplifying the LO frequency signal prior to multiplying the LO frequency signal to the IF signal in the mixer, element number 77 (Column 7, lines 4-10). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to add Moe et al.'s LO amplifier to Merenda's transmitter in order to amplify the LO signal and thus enhancing the quality of the mixer and transmitter.

6. Claims 11 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merenda. The transmitter and method of Merenda is described above in the discussion of claims 9 and 22. Merenda in figure 4c teaches the use of two diode ring arrays arranged in parallel to form a diode ring array (Column 8, lines 37-42). It would be obvious to one of ordinary skill in the art at the time of the applicant's invention to increase it to four diode rings since adding more diode rings in parallel will not produce an unexpected result since the product of two diode rings in parallel has been taught.

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Merenda and Joshi further in view of Kaiser (U.S. 5,339,284). The modified transmitter of Merenda and Joshi is described above in the discussion of claim 16. Merenda and Joshi do not disclose the filter specifically being a triplexer. However, Kaiser discloses

using a triplexer as a filter at the output of a mixer (Column 9, lines 28-38). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention, to apply Kaiser's filtering technique with the use of a triplexer to the modified transmitter of Merenda and Joshi in order to specifically isolate three relevant frequencies.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Vaisanen (U.S. 5,379,458) discloses a diode mixer. Itoh et al. (U.S. 5,787,126) discloses a detector mixer circuit that utilizes a parallel diode circuit. Sadhir (U.S. 5,428,840) discloses a diode mixer circuit with filters at both the input and output. Martinson et al. (U.S. 5,446,923) discloses a harmonic diode mixer utilizing anti-parallel diode circuitry.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adeel Haroon whose telephone number is (571) 272-7405. The examiner can normally be reached on Monday thru Friday, 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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5/11/05

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